AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said delay analysis system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library,

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information comprising delay time information for a signal path from input terminals to output terminals of a logical circuit of said at least one circuit, wherein the delay time information is specific to an input terminal logical state transition of the logical circuit and resulting logical state transition at an output terminal of the logical circuit, and wherein said delay time information for each signal path of the logical circuit of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to the logical operation information,

wherein the delay analyzing module automatically analyzes the delay of the logical circuit based on the delay time information in said delay analysis library.

2. (previously presented): A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library,

wherein, for each of said plurality of circuits, said library further comprises respective logical operation information comprising respective delay time information for a signal path from input terminals to output terminals of a respective logical circuit of each of said plurality of circuits, wherein the respective delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for the respective logical circuit of each of said plurality of circuits, and wherein said delay time information for each signal path of said plurality of circuits is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to the respective logical operation information for each of said plurality of circuits,

wherein the delay analyzing module automatically analyzes the delay of the respective logical circuit of each of said plurality of circuits based on the respective delay time information in said delay analysis library.

3. (currently amended): A computer-implemented method of making a delay analysis of a logic circuit, comprising:

referencing, using a computer, a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information for said plurality of the circuits, wherein the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, said delay time information for each signal path of said logical circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for said at least one circuit; and

automatically selecting a delay time of each path of said logical circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information.

4. (previously presented): A computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for

executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

referencing a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information for said plurality of the circuits, wherein the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, said delay time information for each signal path of said logical circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for said at least one circuit;

automatically selecting a delay time of each path of said logical circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information; and

performing a delay calculation to determine a propagation delay time of the at least one circuit using said selected delay time of said logical circuit.

5. (previously presented): The delay analysis system as set forth in claim 1, wherein the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed.

6. (previously presented): The delay analysis system as set forth in claim 5, wherein the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case.